

HOT CHIPS 21

..... The 21st annual Hot Chips conference was held in August 2009 at Stanford University. Hot Chips has emerged as the leading forum to present new processor architectures and other developments in chip design, with an emphasis on deep technical discussion of the detailed workings of upcoming commercial products. A few selected presentations from leading academic researchers complement the industry focus.

To encourage busy industry engineers to submit to the conference, the submission guidelines require only a short abstract and the conference proceedings contain only the presentation slides. In addition, a few of the authors are asked to submit full-length papers for consideration for publication in this special issue of *IEEE Micro*. From more than 75 submissions, the program committee selected 27 presentations for the main conference. This special issue contains seven full-length articles representing the important themes discussed at the conference.

Multicore server processors

Multicore processors were again a pervasive theme at Hot Chips, and this year, presentations included several high-end server processors.

In "Power7: IBM's Next-Generation Server Processor," Ron Kalla and his colleagues present architectural details of IBM's latest server processor, which has eight powerful out-of-order cores and a large embedded DRAM cache on chip.

In "Cache Hierarchy and Memory Subsystem of the AMD Opteron Processor," Pat Conway and his colleagues introduce the latest "Magny Cours" incarnation of the AMD Opteron architecture. The "Magny

Cours" chip features a reconfigurable coherence scheme to trade some last-level cache capacity to enable scaling of the coherence scheme to systems with 48 cores.

Finally, in "Sparc64 VIIIfx: A New-Generation Octocore Processor for Petascale Computing," Takumi Maruyama and his colleagues describe Fujitsu's new eight-core Sparc-compatible processor designed for high-end scientific computing.

Ubiquitous parallel computing

Parallel hardware continues to advance rapidly, with the introduction of multicore and many-core processors into all types of computer systems, but this has created perhaps the most difficult programming challenge in software's history. How will most programmers be able to effectively use all of these parallel cores given the long history of failed parallel computing efforts?

The three current leading academic centers of parallel computing research—the University of California, Berkeley, the University of Illinois, and Stanford University—presented their latest progress on tackling this programming challenge in a special session at the conference, which included a joint panel that took questions from the audience. The conference attendees voted this session the favorite of the conference, and so we invited the three centers to prepare a single joint article "Ubiquitous Parallel Computing from Berkeley, Illinois, and Stanford" that compares and contrasts their approaches.

Accelerators

Another theme in the industry is the use of accelerators to provide higher performance



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or better energy efficiency than conventional processors. One of the conference keynotes was from Jen-Hsun Haung, CEO of NVIDIA, who described "The GPU Computing Era." The included article by John Nickolls and William J. Dally captures the keynote theme but also adds details of the latest Fermi architecture, which has greatly extended general-purpose capabilities compared to earlier NVIDIA GPUs.

Another article, "Instruction Set Innovations for the Convey HC-1 Computer," by Tony M. Brewer, describes the Convey HC-1 heterogeneous computer, which adds a field-programmable gate array-based coprocessor and high-performance memory system to an industry-standard Intel processor. The coprocessor can be configured with a custom instruction set to provide high-performance processing tailored to an application domain.

MEMS oscillators

Hot Chips is not only about processors. The conference also seeks out interesting technologies that will impact future chip designs. In "Silicon MEMS Oscillators for High-Speed Digital Systems," Sassan Tabatabaei and Aaron Partridge describe the use of the resonance properties of microelectromechanical systems to provide high-quality clock sources for digital systems.

Although we could only include these few articles in the special issue, the full set of presentation slides for this year and all previous years of Hot Chips is available online at <http://www.hotchips.org>.

We hope you enjoy this special issue and look forward to seeing you at Hot Chips 22!

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